

	L #	Hits	Search Text	DBs	Time Stamp
1	L1	130	(438/249) .CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 11:08
2	L2	243465 08	((@ad<"20030917") or (@rlad<"20030917"))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 11:09
3	L3	122	1 and 2	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 11:11

	L #	Hits	Search Text	DBs	Time Stamp
4	L4	77	3 and ("silicon nitride" or SiN)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 12:34
5	L5	8	("6008104"   "6018174"   "6265741"   "6310375"   "6319788"   "6362040"   "6417064"   "6551875").PN.	US- PGPUB; USPAT; USOCR	2005/04/24 11:14
6	L6	0	("6821844").URPN.	USPAT	2005/04/24 11:15
7	L7	99	(438/392).CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 12:34
8	L8	94	7 and 2	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 12:42

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9	L9	94	(438/561).CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 12:42
10	L10	84	9 and 2	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 12:43
11	L11	38	10 and ("silicon nitride" or SiN)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 14:04

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12	L12	617	(438/386).CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 14:05
13	L13	585	12 and 2	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 14:05
14	L14	377	13 and ("silicon nitride" or SiN)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 14:20
15	L15	1328	"doped silicate glass"	US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 14:20

	L #	Hits	Search Text	DBs	Time Stamp
16	L16	529	((deposit\$6 or fill\$6) near4 (SiN or "silicon nitride") near8 (opening or trench)) and (DRAM or "dynamic random access memory")	US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 14:21
17	L17	4	14 and 15 and 16	US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 14:29
18	L18	2	("6,316,310").PN.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/04/24 14:29

US-PAT-NO: 6319787

DOCUMENT-IDENTIFIER: US 6319787 B1

TITLE: Method for forming a high surface area trench capacitor

----- KWIC -----

Application Filing Date - AD (1):

19980630

Brief Summary Text - BSTX (2):

This invention relates generally to trench capacitors and more particularly to trench capacitors adapted for use with Dynamic Random Access Memories (DRAMs).

Brief Summary Text - BSTX (3):

As is known in the art, a challenge in current DRAM technology is to provide smaller and smaller feature sizes to thereby increase the number of storage cells in a given surface space of a chip and yet provide such storage cell with a capacitor of sufficient size to store, and maintain, a requisite amount of charge. One approach currently being investigated is to use dielectric materials for the capacitor having high dielectric constants. Other approaches seek to enhance the total surface area of the capacitor structure by modifying the geometrical layout of the storage cell.

Drawing Description Text - DRTX (3):

FIG. 1 is a diagrammatical cross-sectional sketch of a DRAM cell having a trench capacitor according to the invention;

Drawing Description Text - DRTX (4):

FIG. 2 is a cross-sectional of a portion of the DRAM cell capacitor of FIG. 1, such cross-section being taken along line 2--2 in FIG. 1;

Detailed Description Text - DETX (2):

Referring now to FIGS. 1 and 2, a DRAM cell 10 is shown formed in

a silicon substrate 12, here having p.sup.+ type doping conductivity. The DRAM cell 10 includes a MOSFET 14 connected to a capacitor 16. The capacitor 16 is a trench capacitor. A conductive material 20, here p.sup.+ type conductivity doped polycrystalline silicon, is disposed within the trench in a manner to be described, to provide a first electrode of the capacitor 16. A first dielectric material 22, here silicon nitride is disposed, in a manner to be described, on sidewalls of the conductive material 20. Another conductive material 24, here n type conductivity doped polycrystalline silicon, is disposed, in a manner to be described, on the first dielectric material 22 to provide a second electrode for the capacitor 16. A second dielectric material 26, here also silicon nitride, is disposed between the conductive material 24 and the sidewalls of the trench in a manner to be described. Here, the substrate 12 has a conductive region therein, here the p.sup.+ type conductivity substrate, and the first electrode provided by conductive material 20 is in electrical contact with the conductive region, i.e., here the substrate 12.

Detailed Description Text - DETX (6):

A dielectric collar 42, here silicon dioxide, is formed at the upper portion of the trench, as indicated. The collar 42 prevents leakage of the "node junction" 38, and strap 40 to the buried plate, here provided by the p.sup.+ substrate 12. Leakage is undesirable as it degrades the retention time of the DRAM cell 10, increasing the refresh frequency which adversely impacts performance.

Detailed Description Text - DETX (7):

A buried well, not shown, comprising n-type dopants, such as phosphorous or arsenic, may be provided below the surface of the substrate 10. The buried well serves to connect the buried plates of other DRAM cells in an

array, not shown. A Shallow Trench Isolation (STI) 46 is provided to isolate the DRAM cells, not shown, formed in the substrate 12.

Detailed Description Text - DETX (8):

Referring now to FIGS. 3A-3I, the method for forming the trench capacitor 16 (FIGS. 1 and 2) will be described. Thus, referring to FIG. 3A, the silicon, semiconductor p.sup.+ type conductivity substrate 12 is provided. Here the substrate 12 has a p type conductivity epitaxial layer 36. A pad stack 74 of a lower layer 74a of thermally formed silicon dioxide, an intermediate layer 74b of low pressure chemical vapor deposited silicon nitride, and an upper layer 74c of oxide, for example low pressure chemically vapor deposited TEOS or borosilicate doped glass (BSG), is formed on the surface of the silicon substrate 10. As noted above, the substrate 12 is doped with p type conductivity dopant, here (p.sup.+), such as boron. The substrate 12 has the more lightly doped p type conductivity epitaxial layer 36. The pad stack 74 is patterned using conventional photolithography to define a region in which a trench 37 for the capacitor is to be formed.

Detailed Description Text - DETX (9):

After forming the trench 37, here using a plasma etching process, in the substrate 12, as shown, the sidewalls of the trench 37 are lined with low pressure chemically vapor deposited silicon nitride layer 25, here to a thickness of about 5 nanometers (nm), as shown in FIG. 3B. It should be noted that any type of nitride may be used which can be deposited with sufficient conformality.

Detailed Description Text - DETX (10):

Next a sacrificial material 27, here chemically vapor deposited phosphorus doped silicate glass (PSG), or other doped silicate glass is deposited over the surface of the layer 25, as shown in FIG. 3B. A plasma etch



(reactive ion etch, RIE, here using a CF.sub.4 combined with CHF.sub.3 and argon) is used to remove bottom portions of the PSG material 27 and the silicon nitride layer 25, as shown in FIG. 3B.

Detailed Description Text - DETX (13):

Referring now to FIG. 3F, a wet etch, here for example, an hydrofluoric acid based etch, is used to selectively remove the sacrificial PSG material 27. It is noted that other oxides may be used which have enough selectivity for the deep trench etching step and which can be removed by a wet etch. Thus, the oxide may be any type which exhibits high wet etch selectivity to doped polycrystalline silicon and nitride.

Detailed Description Text - DETX (14):

It is noted that, referring again to FIG. 3D, after the upper portions of the p.sup.+ doped polycrystalline silicon 20 are removed, the upper portions of the silicon nitride layer 25 and the upper portions of the sacrificial layer 27 may be removed using chemical mechanical polishing or reactive ion etching thereby exposing the TEOS or BSG layer 74c. Then, a wet etch, here for example, an hydrofluoric acid based etch, is used to selectively remove any remaining portions sacrificial PSG material 27. The upper portions of the polycrystalline silicon 20 are then recess etched.

Detailed Description Text - DETX (15):

Referring to FIG. 3G, if the silicon nitride layer 25 is not removed, as described above, a wet etch is used to remove the silicon nitride layer 25. The TEOS/BSG mask 74c (FIG. 3A) is etched away. In either case, after removal of any remaining PSG sacrificial material 27, it is noted that the silicon sidewalls 29 of the trench and peripheral portions 31 of the conductive material, i.e., the doped polycrystalline silicon 20, have an open region 33